Amendments to the Claims:

1. (Currently Amended) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

forming at said ingress processor a header for each frame destined for said egress processor said header having code for identifying a beginning address of picocode instructions stored in said egress processor and data, generated by said ingress processor, to be used as required by said picocode instructions being executed; and

decoding said code in said header in a hardware frame classifier into a starting address in said picocode for said egress processor.

2. (Original) The method for enhancing processing according to claim 1 wherein said frame header includes control information for said egress processor which distinguish said frames as being multicast or unicast.

3. (Currently Amended) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

forming at said ingress processor a header for each frame destined for said egress processor having code for identifying a beginning address of picocode instructions stored in said egress processor and data, generated by said ingress processor, to be used as required by said picocode instructions being executed; and

decoding said code in said header in a hardware frame classifier into a starting address in said picocode for said egress processor wherein decoding said code include indexing an address table in said hardware frame classifier; and executing processing from a starting address space identified by said table of said hardware classifier.

4. (Previously Presented) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed comprising:

forming at said ingress processor a header for each frame destined for said egress processor having data for identifying a beginning of a processing sequence for said egress processor; and

decoding said data in said header in a hardware frame classifier into a starting address for said egress processor wherein decoding said data include indexing an address table in said hardware frame classifier; and executing processing from a starting address space identified by said table of said hardware classifier if said hardware classifier is enabled and executing processing of said frame beginning at a process execution level determined from a port configuration entry of the interface of the port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled.

5. (Original) The method for enhancing processing according to claim 1 wherein said egress processor creates multiple frames for multiple output ports when said frame header contains multicast data.

6. (Currently Amended) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress

processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

forming at said ingress processor a header for each frame destined for said egress processor having code for identifying a beginning address of picocode stored in said egress processor and data, generated by said ingress processor, to be used as required by said picocode instructions being executed; and

decoding said code in said header in a hardware frame classifier into a starting address in said picocode for said egress processor wherein a parameter is encoded into a field of said frame header by said ingress processor which is read by a picocode instruction executed by said egress processor.

7. (Currently Amended) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed comprising:

forming at said ingress processor a header for each frame destined for said egress processor having ~~data~~ code for identifying a beginning of a processing sequence for said egress processor and data inserted by said ingress processor to be used by said egress processor as required by picocode instructions in said egress processor; and

decoding said data in said header in a hardware frame classifier into a starting address for said egress processor wherein decoding said data include indexing an address table in said hardware frame classifier; and executing processing from a starting address space identified by said table of said hardware classifier wherein said data is located in two fields, the first of which identifies the number of bytes in a second field containing parameters for execution by said egress processor.

8. (Currently Amended) A network switch for enhancing execution of frame classification information comprising:

an ingress processor for parsing and recovering parameters from a frame and recovering the identity of said frame;

said ingress processor being further programmed to create a header for an intra-switch frame identifying said frame and a level of processing of said received frame including data inserted by said ingress processor to be used by said egress processor as is required by picocode instructions in said egress processor;

an egress processor for receiving said intra-switch frame and for creating a frame for passing to one or more output ports, said egress processor being programmed to:

execute instructions which follow a starting address for completing processing of said frame;

forward said processed frame to an output port based on said processing of said frame; and

a hardware frame classifier for determining from said intra-switch frame header said starting address of said instructions which are to be processed wherein the level of processing of said received frame includes code for identifying a beginning address of picocode instructions stored in said egress processor and data generated by said ingress processor, to be used as required by said pico instructions being executed.

9. (Currently Amended) ~~The network switch according to claim 8 wherein said hardware frame classifier~~ A network switch for enhancing execution of frame classification information comprising:

an ingress processor for parsing and recovering parameters from a frame and recovering the identity of said frame;

said ingress processor being further programmed to create a header for an intra-switch frame identifying said frame and a level of processing of said received frame;

an egress processor for receiving said intra-switch frame and for creating a frame for passing to one or more output ports, said egress processor being programmed to:

execute instructions which follow a starting address for completing processing of said frame;

forward said processed frame to an output port based on said processing of said frame; and

a hardware frame classifier, includes an address table which decodes frame header extension values and variable frame extension values which point to said egress processor starting address location, for determining from said intra-switch frame header said starting address of said instructions which are to be processed wherein the level of processing of said received frame includes code for identifying a beginning address of picocode instructions stored in said egress processor and data generated by said ingress processor, to be used as required by said pico instructions being executed.

10. (Currently Amended) A network switch for enhancing execution of frame classification information comprising:

an ingress processor for parsing and recovering parameters from a frame and recovering the identity of said frame;

said processor being further programmed to create a header for an intra-switch frame identifying said received frame and a level of processing of said received frame wherein said header includes a field which identifies the number of bytes in a variable length field which contain parameters determined by said ingress processor;

an egress processor for receiving said intra-switch frame and for creating a frame for passing to one or more output ports, said egress processor being programmed to:

execute instructions which follow a starting address for completing processing of said frame;

forward said processed frame to an output port based on said processing of said frame; and

a hardware frame classifier for determining from said intra-switch frame header said starting address of said instructions which are to be processed.

11. (Original) The network switch according to claim 8 wherein said frame header includes a field to identify said received frame as being a multicast frame.

12. (Previously Presented) The network switch according to claim 8 wherein said frame header is stored in fixed length fields which have a length determined by a length field in said header.

13. (Currently Amended) In a network switch which receives frames of data on a set of input ports and delivers said frames to an output port, a method for improving frame processing time comprising:

partially processing a received frame in an ingress processor which parses said received frame ~~parameters~~ and prepares an intraswitch frame for delivery to an egress processor associated with said output port; said ingress processor creating a header for said intraswitch frame having a data for identifying parameters computed by said ingress processor and code for identifying a starting address for said egress processor; and

completing processing of said frame in an egress processor which receives said intraswitch frame and passes said processed frame to an output port, said

egress processor completing processing from program instructions which have a starting address defined by said header data and from parameters computed by said ingress processor, whereby processing performed by said ingress processor is not unnecessarily performed by said egress processor.

14. (Original) The method for improving frame processing according to claim 13 wherein said ingress processor encodes in said header data representing a level of processing completed by said ingress processor.

15. (Original) The method for improving frame processing according to claim 13 wherein said ingress processor creates multiple fields in said header for indicating the type of frame received, and for indicating the level of processing completed by said ingress processor.

16. (Original) The method for improving frame processing according to claim 13 wherein a hardware classifier identifies said starting address from said identifying data in said header.

17. (Previously Presented) The method for improving frame processing according to claim 16 wherein said hardware classifier locates said address from table which is indexed by said identifying data.

18. (Original) The method for improving frame processing according to claim 13 wherein said egress processor is programmed to detect a multicast bit contained in said frame header which identifies said frame as being destined to multiple ports.

19. (Previously Presented) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress

processor having a port through which said frames are delivered, a method for enhancing processor speed comprising:

forming at said ingress processor a header for each frame destined for said egress processor said header having data identifying parameters computed by said ingress processor and code identifying a starting address of picocode instructions stored in said egress processor wherein the data identifying parameters is to be used as required by the picocode instruction being executed; and

decoding said code in said header in a hardware frame classifier into the starting address in said picocode for said egress processor.

20. (Currently Amended) A method for processing data comprising:

generating in an ingress processor a header having code identifying a starting address of picocode instructions stored in an egress processor whereat said egress processor is to begin when processing and data inserted by said ingress processor to be used by said egress processor as is required by said picocode instruction;

appending the header to a frame routed to the egress processor by said ingress processor;

receiving the header in said egress processor; and

processing the frame according to the picocode instructions beginning at the starting address of said picocode instructions set wherein said egress processor expedites its processing speed by utilizing data resulting from earlier processing performed by the ingress processor.

21. Cancelled.

22. (Currently Amended) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress

processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

forming at said ingress processor a header for each frame destined for said egress processor said header having ~~data~~ parameter for identifying a beginning of a processing sequence for said egress processor, data, generated by said ingress processor, to be used as required by said processing sequence and control information for said egress processor which distinguish said frames as being multicast or unicast; and

decoding said data in said header in a hardware frame classifier into a starting address for said egress processor.

23. (Previously Presented) The method of claim 22 wherein the control information includes a single bit when set to a first state indicates the unicast frame and when set to a second state indicates the multicast frame.

24. (Currently Amended) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

forming at said ingress processor a header for each frame destined for said egress processor having ~~data~~ code for identifying a beginning of a processing sequence for said egress processor, data, generated by said ingress processor, to be used as required by said processing sequence;

decoding said data in said header in a hardware frame classifier into a starting address for said egress processor; and

creating multiple frames for multiple output ports when said frame header contains multicast data.

25. (Previously Presented) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

forming at said ingress processor a header for each frame destined for said egress processor said header having code for identifying a beginning address of picocode instructions stored in said egress processor; and

decoding said code in said header in a hardware frame classifier into a starting address in said picocode for said egress processor if said classifier is enabled otherwise executing processing of a frame beginning at a process execution level determined from a port configuration entry of the interface of the port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled.

26. (Previously Presented) The method for enhancing processing according to claim 25 wherein said frame header includes control information for said egress processor which distinguish said frames as being multicast or unicast.

27. (Currently Amended) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

forming at said ingress processor a header for each frame destined for said egress processor having code for identifying a beginning address of picocode stored in said egress processor; and

decoding ~~said~~ data in said header in a hardware frame classifier into a starting address in said picocode for said egress processor wherein decoding said code include indexing an address table in said hardware frame classifier; and

executing processing from a starting address space identified by said table of said hardware classifier if said hardware classifier is enabled, otherwise executing processing of a frame beginning at a process execution level determined from a port configuration entry of the interface of the port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled.

28. (Previously Presented) The method for enhancing processing according to claim 25 wherein said egress processor creates multiple frames for multiple output ports when said frame header contains multicast data.

29. (Currently Amended) A network switch for enhancing execution of frame classification information comprising:

an ingress processor for parsing and recovering parameters from ~~said~~ a frame and recovering the identity of said frame;

said ingress processor being further programmed to create a header for an intra-switch frame identifying ~~said~~ a received frame and a level of processing of said received frame;

an egress processor for receiving said intra-switch frame and for creating a frame for passing to one or more output ports, said egress processor being programmed to:

a hardware frame classifier for determining from said intra-switch frame header ~~said~~ a starting address of said instructions which are to be processed;

executing processing of a frame beginning at a process execution level determined from a port configuration entry of the interface of ~~the~~ a port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled; and

forward said processed frame to an output port based on said processing of said frame.

30. (Previously Presented) The network switch according to claim 29 wherein said hardware frame classifier includes an address table which decodes frame header extension values and variable frame extension values which point to said egress processor starting address location.

31. (Currently Amended) The network switch according to claim 29 wherein said frame header includes a field to identify said ~~received~~ frame as being a multicast frame.

32. (Previously Presented) The network switch according to claim 29 wherein said frame header data is stored in fixed length fields which have a length determined by a length field in said header.

33. (Previously Presented) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed comprising:

forming at said ingress processor a header for each frame destined for said egress processor said header having data identifying parameters computed by said ingress processor and code identifying a starting address of picocode instructions stored in said egress processor; and

decoding said code in said header in a hardware frame classifier into the starting address in said picocode for said egress processor if said classifier is enabled otherwise executing processing of a frame beginning at a process execution level determined from a port configuration entry of the interface of the

port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled.

34. (Currently Amended) A method for processing data comprising:

generating in an ingress processor a header having code identifying a starting address of picocode instructions stored in an egress processor whereat said egress processor is to begin when processing and data inserted by said ingress processor to be used by said egress processor as is required by said picocode instruction;

appending the header to a frame routed to the egress processor by said ingress processor;

receiving the header in said egress processor; and

processing the frame according to the picocode instructions beginning at a process execution level determined from a port configuration entry of the interface of the port said frame was received.

35. Cancelled.

36. (Currently Amended) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

forming at said ingress processor a header for each frame destined for said egress processor said header having data for identifying a beginning of a processing sequence for said egress processor and control information for said egress processor which distinguish said frames as being multicast frame or unicast frame; and

decoding said data in said header in a hardware frame classifier into a starting address for said egress processor if said classifier is enabled otherwise executing processing of a frame beginning at a process execution level determined from a port configuration entry of the interface of the port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled.

37. (Previously Presented) The method of claim 36 wherein the control information includes a single bit when set to a first state indicates the unicast frame and when set to a second state indicates the multicast frame.

38. (Previously Presented) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

forming at said ingress processor a header for each frame destined for said egress processor having data for identifying a beginning of a processing sequence for said egress processor;

decoding said data in said header in a hardware frame classifier into a starting address for said egress processor if said classifier is enabled otherwise executing processing of a frame beginning at a process execution level determined from a port configuration entry of the interface of the port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled; and

creating multiple frames for multiple output ports when said frame header contains multicast data.